Switching Strategies Based Cascaded Multilevel Inverters Using Modulation Techniques

S.Kannadhasan¹, M.Saravanapandi², C.Gurunathan³

^{1,3}Lecturer, ²Senior Lecturer
Department of Electrical and Electronics Engineering,
^{1,3}Tamilnadu Polytechnic College, Madurai, Tamilnadu, India,
²Latha Mathavan Polytechnic College, Madurai, Tamilnadu, India.

ABSTRACT: This paper presents four different sequential switching hybrid-modulation strategies cascaded multilevel inverters. Hybrid-modulation strategies represent combinations of fundamental-frequency modulation and multilevelsinusoidal-modulation (MSPWM) strategies, and are designed forperformance of the well-known alternative phase opposition disposition, phase-shifted carrier, carrier-based space-vector modulation, and single-carrier sinusoidal-modulations. The main characteristicof thesemodulations are the reduction of switching losseswith good harmonic performance, balanced power loss dissipationamong the devices with in a cell, and among the series-connected cells. The proposed modulations can be easily extended to three phase, and higher level inverters, operates with same physical structure of the power module. The feasibility of these hybrid modulations are verified through simulation, and experimental results.

Keywords: Cascaded multilevel inverter (CMLI), hybridmodulation.

I.INTRODUCTION

MULTILEVEL inverters (MLIs) have increased attention in industries as a choice of electronic powerconversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation [1].Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion and can operate on several voltage levels. Various multilevel inverter (MLI) structures are reported in the literature, and the cascaded MLI (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI) [2]. Other conventional MLIs have some disadvantages like more storage capacitors and clamping diodes.



Fig. 1.Schematic diagram of the proposed hybrid modulations

Most of the modulation methods developed for MLI isbased on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with verticalshifts (phase disposition, phase opposition disposition, and alternativephase opposition disposition (APOD) PWM), or withhorizontal displacements (phase-shifted carrier (PSC) PWM)[5]. Space-vector modulation (SVM) is also extended for theMLI operation, offers good harmonic performance [6]. These high-frequency methods produce high-frequency stepped voltagewaveforms that are easily filtered by the load and, therefore, present very good reference tracking and low current harmonic distortion. However, this is also the reason for high switchinglosses, which is undesirable in high-power applications. As aresult, fundamental-frequency modulation methods have been preferred. Selective harmonic elimination (SHE) has the advantageof having very few commutations per cycle and is, therefore, the one that achieves better

efficiency [7]. SHE becomes unfeasible with the increase of the number of levels, since it is directly related to the number of angles, hence equations that need to be solved.

This paper addresses the issue to reduce the switching loss of multilevel sinusoidal-modulation (MSPWM) schemes withlow computational overhead. Also, it covers the methodologyfor equal power dissipation among the power devices, and thepower modules. The proposed method can be equally applied to any number of voltage levels, any number of phases, and switching transitions.

II. PROPOSED METHOD

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation, so that the output inherits the features of switching loss reduction from FPWM, and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; twobeing commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequalswitching losses and therefore differential heating among the power devices. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makesbalanced power dissipation among the power modules.



Fig.2. Scheme of proposed sequential switching hybrid modulation

The general structure of the proposed SSHM scheme consists of modulation base generator, base PWM circulation module, and generate hybrid modulation controller (HMC) to new modulation pulses. In this modulation strategy, three base modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (A) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (B) is a square wave signal synchronized with the modulation waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during negative half cycle. A sequential switching pulse (SSP) and FPWM pulses are same for all inverter cells. MSPWMs (C or D) for each cell, differs depends upon the type of carrier and modulation signals used. The block diagram representation of base modulator design is shown fig.3 (a)-(d)

Fig.3. Scheme of proposed sequential switching hybrid modulation

APOD modulation pulses for cell-I (C) is obtained from the comparison between unipolar modulation waveform and carrier, while APOD for cell-II (D) is generated from the comparison between modulation waveform and carrier with DC bias of -V_c+ $2A_C$. The modulation signals with DC bias of -A_C are compared with single carrier to define **SCSPWM** pulses. CBSVM is based on a comparison of the modified sinusoidal reference $(V_a + V_{off} + V'_{off})$ with each carrier to determine the voltage



level that the inverter should switch to. A PSC pulses are based on the comparison of modulation waveform with the corresponding PSC waveform for every cell in a CMLI.

A simple base PWM circulation scheme introduced here to get resultant HPWM circulation among the power modules. The scheme of five-level base PWM circulation is shown in Fig. 5, consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is fo/4, makes the time base for PWM circulation from one module to another. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module, the second becomes the third, etc., while the last module HPWM shifts to the first.



Fig.5 Five-level base PWMCirculation

HMC combines SSP, FPWM, and MSPWM that producesSSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

 $S_1 = ABC' + \overline{A}B$ $S_2 = \overline{A}BC' + \overline{A}\overline{B}$ $S_3 = \overline{A}\overline{B}C' + A\overline{B}$ $S_4 = \overline{A}BC' + AB$ And $S'_1 = ABD' + \overline{A}B$

 $S'_{2} = \overline{A}BD' + \overline{A}\overline{B}$ $S'_{3} = \overline{A}\overline{B}D' + A\overline{B}$

 $S'_4 = \overline{A}BD' + AB$

Where

A = Sequential signal

B = Fundamental Frequency Pulse Width Modulation

C or D=Multiple Sinusoidal pulse Width Modulation

Capability and switching losses of each gate pulse is composed of both FPWM and MSPWM. If SSP A = 1, then S1, S2, S1', and S2'are operated with MSPWM, while S3, S4, S3', and S4' are operated at FPWM. If SSP A = 0, then S1, S2, S1', and S2'are operated at FPWM, while S3, S4, S3', and S4'are operated with MSPWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module (S1, S2, S3, and S4) becomes the second module (S1', S2', S3', and S4'), and the second one shifts to the first, and is shown in Fig. 6. It can be observed from the waveforms of Vh1 and Vh2 that the implementation of HPWM circulation makes the inverter modules operate at same average switching frequency with the same conduction period. As a result, all inverter cells operate in a balanced condition with the same power-handling capability and switching losses.

Thus the resultant inverter switching is same as the type of MSPWM used. In addition to that, the FPWM operates in parallel with MSPWM, this leads to the switching frequency of the power devices being reduced. Thus their switching losses also decrease.

III.SIMULATION RESULTS DISCUSSION

In order to verify that the proposed modulation can be practically implemented in a cascaded multilevel inverter, simulations were performed using MATLAB/Simulink. The voltage waveform with FFT analysis and five level output phase voltage waveform are shown in fig.6 and fig.7 respectively



Fig.6.Spectrum of the phase voltage waveform



Fig.7 Five level output phase voltage waveform



Fig.8 Speed and Torque waveform **IV.CONCLUSION**

A sequential switching hybrid modulation technique for cascaded multilevel inverter, operating at a lower switching frequency has been obtained. This technique is applied to well-known MSPWM schemes; POD, PSC, CBSVM, and SCSPWM. Compared to conventional MSPWM schemes, less number of commutations and considerable switching-loss reduction is obtained. The harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good. An efficient sequential switching and PWM circulation techniques are embedded with these hybrid modulations for balanced power dissipation among the power devices within a cell and for series connected cells.

REFERENCES

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] J. Rodr'iguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] M.Malinowski, K. Gopakumar, J. Rodr'iguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1047–1058, Mar. 2008.

[5] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858–867, Aug. 2002.

[6] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three-phase converters," IEEE Trans. Ind. Appl., vol. 37, no. 2, pp. 637–641, Mar. 2001.

[7] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 459–469, Mar. 2006.

[8] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral point clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 294–304, Feb. 2009.